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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,381	01/05/2001	Evelyn Duesterwald	10990963-1	5203

22879 7590 01/21/2005

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EXAMINER	
YIGDALL, MICHAEL J	

ART UNIT	PAPER NUMBER
2122	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,381	DUESTERWALD ET AL.	
	Examiner	Art Unit	
	Michael J. Yigdall	2122	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 4, 2004 has been entered. Claims 21-42 are now pending.

Response to Arguments

2. Applicant's arguments have been fully considered but they are not persuasive.

3. Applicant contends that Srivastava fails to disclose or suggest identifying each register that is assigned before being read in a second code fragment, and particularly that there is nothing in Srivastava that discloses or suggests that the identified live variables are used to identify which registers are assigned in a block before being used (Applicant's remarks, pages 7-8). Applicant further contends that Srivastava necessarily fails to disclose or suggest comparing the registers in the instructions identified as being possibly live in the first code fragment with the identified registers in the second code fragment, and eliminating an instruction in the first code fragment based on the comparison (Applicant's remarks, page 8).

However, Srivastava discloses (1) identifying each register that is assigned before being read in a second code fragment, (2) comparing the registers in the instructions identified as being possibly live in the first code fragment with the identified registers in the second code fragment,

and (3) eliminating an instruction in the first code fragment based on the comparison, as set forth in the claim rejections below, with particular reference to column 10, lines 9-46.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 21-24 and 32-35 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pat. No. 5,999,737 to Srivastava (art of record, "Srivastava").

With respect to claim 21 (new), Srivastava discloses a method for removing dead code in code fragments of a program (see, for example, column 3, lines 6-12, which shows a method for removing dead code, and column 10, lines 9-46, which shows an instance of such dead code removal), comprising:

(a) identifying each instruction assigning a register that is possibly live for a first exit in a first code fragment (see, for example, procedure or code fragment 105 in FIG. 6, and column 10, lines 18-22, which shows identifying an instruction such as block 182 defining or assigning a register R1 that is possibly live for an exit at block 185);

(b) identifying each register that is assigned before being read in a second code fragment having a first entry (see, for example, procedure or code fragment 104 and entry 174 in FIG. 6,

and column 10, lines 23-25, which shows identifying a register R1 that is restored or assigned before being read);

(c) at a time when linking the first exit from the first code fragment to the first entry in the second code fragment, comparing the registers in the instructions identified as being possibly live in the first code fragment with the identified registers in the second code fragment (see, for example, column 10, lines 15-28, which shows comparing the registers, and column 2, lines 32-41, which shows operating at link time); and

(d) eliminating an instruction in the first code fragment based on the comparison (see, for example, column 10, lines 28-37, which shows eliminating instructions in procedure or code fragment 105 based on the comparison of registers).

With respect to claim 22 (new), Srivastava also discloses the limitation wherein an instruction identified in the first code fragment is eliminated if the register assigned in the identified instruction matches a register identified in the second code fragment (see, for example, column 10, lines 23-32, which shows that an instruction in procedure or code fragment 105 is eliminated if the registers match).

With respect to claim 23 (new), Srivastava also discloses the limitation wherein an instruction assigning a register is possibly live if there is an exit before the register is reassigned and the exit is before the register is read (see, for example, column 10, lines 18-22, which shows that an instruction assigning a register such as block 184 is possibly live if there is an exit at block 185 before register R1 is reassigned or read).

With respect to claim 24 (new), Srivastava also discloses the limitation wherein an instruction assigning a register is possibly live if the register is not read subsequently in the first code fragment (see, for example, column 10, lines 18-22, which shows that an instruction assigning a register such as block 183 is possibly live if register R2 is not read subsequently in the procedure or code fragment).

With respect to claim 32 (new), the claim recites a computer readable medium that corresponds to the method of claim 21. Srivastava discloses a computer readable medium operable on a computer for removing dead code in code fragments of a program (see, for example, column 3, lines 6-12 and 57-63). The limitations recited in the claim are analogous to those of claim 21 (see Srivastava as applied to claim 21 above).

With respect to claims 33-35 (new), the limitations recited in the claims are analogous to those of claims 22-24 (see Srivastava as applied to claims 22-24 above, respectively).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 25 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava, as applied to claims 21 and 32 above, respectively, in view of U.S. Pat. No. 6,112,025 to Mulchandani et al. (art of record, "Mulchandani").

With respect to claim 25 (new), Srivastava does not expressly disclose the limitation wherein eliminating the instruction comprises overwriting the instruction with a NOP.

However, Mulchandani discloses replacing an instruction with a NOP (see, for example, column 5, lines 30-37) so as to prevent the unwanted effects of executing the instruction (see, for example, column 5, lines 42-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to eliminate the instruction by overwriting the instruction with a NOP, such as taught by Mulchandani, so as to prevent the unwanted effects of executing the instruction.

With respect to claim 36 (new), the limitations recited in the claim are analogous to those of claim 25 (see Srivastava and Mulchandani as applied to claim 25 above).

8. Claims 26 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava, as applied to claims 21 and 32 above, respectively, in view of U.S. Pat. No. 6,041,179 to Bacon et al. (art of record, "Bacon").

With respect to claim 26 (new), Srivastava does not expressly disclose the limitation wherein eliminating the instruction comprises compacting the surrounding instructions to delete the eliminated instruction.

However, Bacon discloses compacting code in a program by linking only the live procedures and not including those determined to be dead (see, for example, column 11, lines 9-13), so as to reduce the code size.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to eliminate the instruction by compacting the surrounding instructions, such as taught by Bacon, so as to reduce the code size.

With respect to claim 37 (new), the limitations recited in the claim are analogous to those of claim 26 (see Srivastava and Bacon as applied to claim 26 above).

9. Claims 27-31 and 38-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava, as applied to claims 21 and 32 above, respectively, in view of U.S. Pat. No. 6,408,433 to Click, Jr. et al. (art of record, "Click").

With respect to claim 27 (new), although Srivastava discloses determining the live ranges of variables so as to remove dead code (see, for example, column 10, lines 1-14), Srivastava does not expressly disclose:

(a) generating a first register mask having a plurality of positions, each position corresponding to a respective register, wherein a bit at a position is set if the respective register is assigned in an instruction identified in the first code fragment; and

(b) generating a second register mask, the second register mask having a plurality of positions, each position corresponding to a respective register, wherein a bit at a position is set if the respective register is one of the identified registers in the second code fragment.

However, Click discloses register masks having a plurality of bit positions, wherein a bit is set if the register corresponding to that bit position is valid (see, for example, column 7, lines 50-53). The register masks are generated so as to determine the live ranges of variables based on the intersection of those register masks (see, for example, column 8, lines 15-22).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to supplement the method of Srivastava with register masks, such as taught by Click, so as to provide an additional means by which to determine the live ranges.

With respect to claim 28 (new), Srivastava in view of Click also discloses the limitation wherein said eliminating step includes eliminating an instruction for assigning a register in the first code fragment if the positions corresponding to the register in the first and second register masks are both set (see, for example, Srivastava, column 10, lines 28-37, which shows eliminating the instructions after determining the live ranges, and Click, column 8, lines 15-22, which shows determining the live ranges based on the intersection of the register masks).

With respect to claim 29 (new), Srivastava also discloses:

(a) identifying each instruction assigning a register that is possibly live for each exit in the first code fragment (see, for example, procedure or code fragment 105 in FIG. 6, and column 10, lines 18-22, which shows identifying an instruction such as block 182 defining or assigning a register R1 that is possibly live for an exit at block 185).

Although Srivastava discloses storing information corresponding to the instructions so as to remove dead code (see, for example, column 10, lines 1-14), Srivastava does not expressly disclose:

(b) storing, in an epilog associated with each exit of the first code fragment, information corresponding to each instruction identified for the corresponding exit.

However, Click discloses using a register allocator to build prolog and epilog code for a calling convention (see, for example, the title, abstract and column 6, lines 38-56), so as to allow

greater flexibility and faster execution (see, for example, column 6, lines 21-25). The calling convention specifies how registers are to be used when procedures are called (see, for example, column 1, line 54 to column 2, line 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to store the information of Srivastava in an epilog, such as taught by Click, so as to allow greater flexibility and faster execution.

With respect to claim 30 (new), Srivastava also discloses:

(a) identifying each register that is assigned before being read after each entry in the second code fragment (see, for example, procedure or code fragment 104 and entry 174 in FIG. 6, and column 10, lines 23-25, which shows identifying a register R1 that is restored or assigned before being read).

Although Srivastava discloses storing information corresponding to the registers so as to remove dead code (see, for example, column 10, lines 1-14), Srivastava does not expressly disclose:

(b) storing, in a prolog associated with each entry of the second code fragment, information corresponding to each register identified for the corresponding entry.

However, Click discloses using a register allocator to build prolog and epilog code for a calling convention (see, for example, the title, abstract and column 6, lines 38-56), so as to allow greater flexibility and faster execution (see, for example, column 6, lines 21-25). The calling convention specifies how registers are to be used when procedures are called (see, for example, column 1, line 54 to column 2, line 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to store the information of Srivastava in an prolog, such as taught by Click, so as to allow greater flexibility and faster execution.

With respect to claim 31 (new), Srivastava also discloses the limitation wherein the information in the corresponding epilogs of the exits in the first code fragment and the information in the corresponding prologs of the entries in the second code fragment are stored prior to the linking of the first exit from the first code fragment to the first entry in the second code fragment (see, for example, column 10, lines 38-46, which shows that the information is stored prior to removing dead code at link time).

With respect to claims 38-42 (new), the limitations recited in the claims are analogous to those of claims 27-31 (see Srivastava and Click as applied to claims 27-31 above, respectively).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. U.S. Pat. No. 5,761,514 to Aizikowitz et al. discloses a register allocation method and apparatus for truncating runaway lifetimes of program variables in a computer system.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael J. Yigdall whose telephone number is (571) 272-3707. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MY

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